IOP4IoT W7500/ W7500P Schematic Design Guide

This is a preliminary document release. All specifications are subject to change without notice.

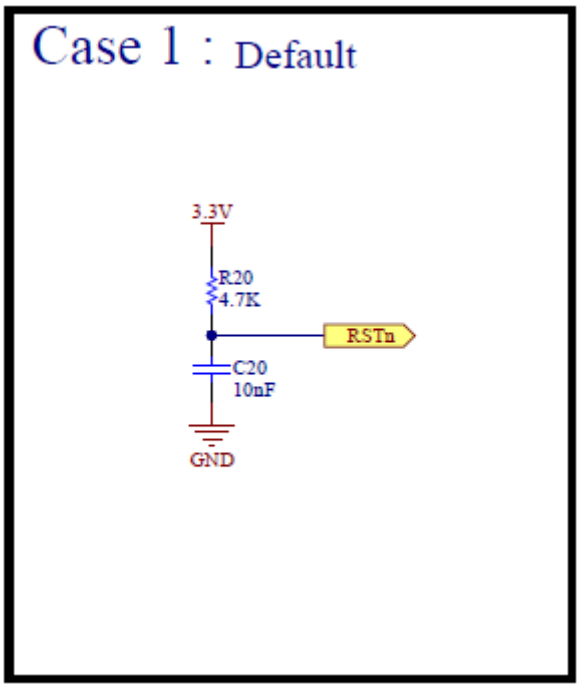
http://www.wiznet.co.kr

These are the reference schematic for W7500/W7500P design; the Reset Pin must be included in the design as below reference schematic files.

W7500	IP Plus PHY	W7500_Ref_Schematic(IC+).PDF
	RealTek PHY	W7500_Ref_Schematic(RT).PDF
W7500P		W7500P_Ref_Schematic.PDF

1. Default

Connect the Reset Pin to the VDD using the pull-up resistance.



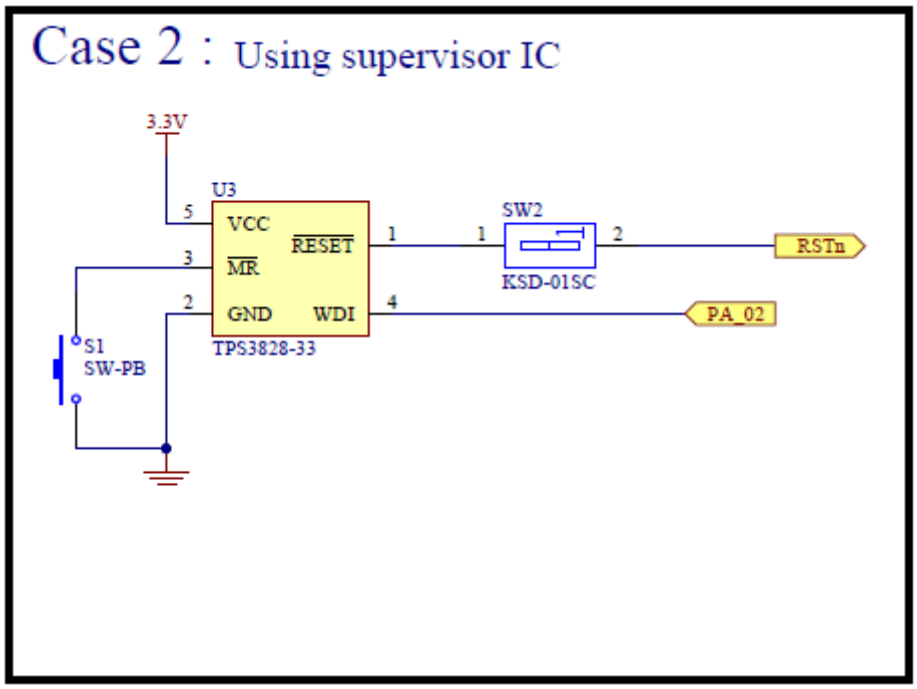
2. Using a Supervisor IC

When using a Reset Switch, a supervisor chip like MAX823, which has watchdog function for monitoring the chip after Reset, is recommended.

- Connect Clock output of PA_02 to WDI.
- Do not Reset using SW1 in ISP mode.

Please include the code below when developing the software.

```
Main()
{
*(volatile uint32_t *)(0x41001170) = 0x0002;    // 8MHz output (125n)
*(volatile uint32_t *)(0x41002008) = 0x0002;    // PAD PA_02 use as CLKOUT
....
}
```



3. Using with another MCU

When using the W7500/W7500P as slave with another master MCU and want to control W7500/W7500P Reset from the master MCU, connect one of the GPIO of the master MCU to the RSTN of W7500/W7500P and connect the other GPIO of the master MCU to the GPIO of W7500/W7500P.
(If there is no need to control W7500/W7500P reset from another master MCU, please design as 1.Default)

Authorize Reset using the GPIO(output) of the MCU and check if the GPIO(input) of W7500/W7500P is operating.

Set the GPIO(PA_02 in below example case) of W7500 as 'high' when developing the software.